Advanced PCB design for EMC

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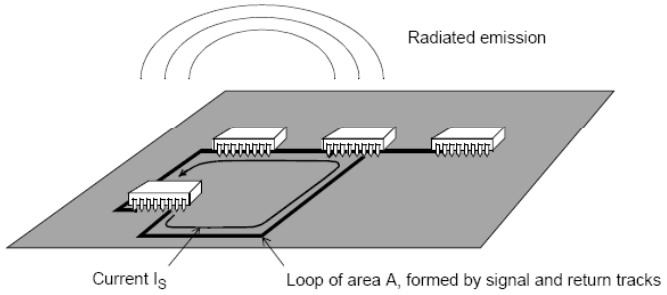
Contents

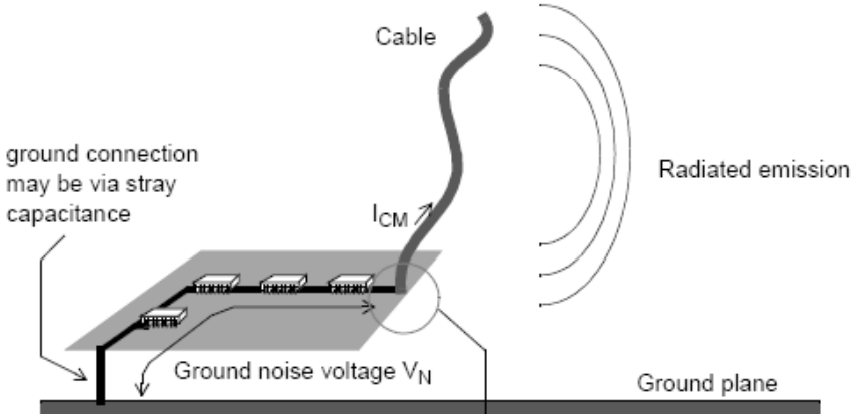
- Introduce EMI Emission on PCB
- Understand current return path in PCB
- Control current return path to reduce EMI.
- Summary

Introduction

☐ Potential Problems on PCB EMI

- ➢ Radiated emission
  - – Differential Mode Emission
  - – Common Mode Emission





Field strength of PCB Emission

- Differential mode Radiated emission

$$E = 131.6 \cdot 10^{-12} (f^2 \cdot A \cdot I_S) / R \cdot \sin\theta \ (V/m)$$

Max. field strength: correcting for ground reflection with a measuring distance of “R (meter)”

$$\mathbf{E} = 263 \cdot 10^{-12} (f^2 \cdot A \cdot I_S) / R \ (V/m)$$

- Common mode Radiated emission

$$\mathbf{E} = 1.26 \times 10{-}4 (f \times L \times I_{CM}) / R \ (V/m)$$

DM Radiated emission from PCB

- $E = 131.6 \cdot 10^{-12} (f^2 \cdot A \cdot I_S) / R \cdot \sin\theta$ (V/m)

Correcting for ground reflection (x2) with a measuring distance of 1m at maximum field strength.

$$E = 263 \cdot 10^{-12} (f^2 \cdot A \cdot I_S) / R \quad (V/m)$$

Example:

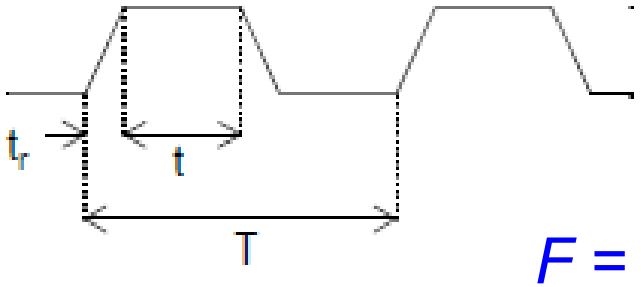
If loop area on PCB is: $A = 10\ cm^2$, $I_S = 20mA$, $f = 50MHz$;

then the Max. emission at 1 m distance is calculated as: $E = 42\ dB\mu V/m$

Example : Maximum loop area on PCB

Logic family	t_r/t_f ns	ΔI mA	Loop area cm^2 at clock frequency 4MHz	10MHz	30MHz	100MHz
4000B CMOS @ 5V	40	6	1000	400	–	–
74HC	6	20	45	18	6	–
74LS	6	50	18	7.2	2.4	–
74ALS	3.5	50	10	4	1.4	0.4
74AC	3	80	5.5	2.2	0.75	0.25
74F	3	80	5.5	2.2	0.75	0.25
74AS	1.4	120	2	0.8	0.3	0.15

Loop area for 30dBμV/m 30MHz–230MHz, 37dBμV/m 230–1000MHz at 10m



F = 30MHz ; T = 33.3ns; (t + tr)/T = 0.5

Maximum loop area on PCB

Example : 74ALS family with F_{clock} = 30MHz,

Assume the **worst case** is at 150MHz (5th harmonic) ;

calculate 5 th harmonic current from source current :

$$I(n) = 2I((t+t_r)/T)\left(\frac{\sin n\pi((t+t_r)/T)}{n\pi((t+t_r)/T)}\right)\left(\frac{\sin n\pi(t_r/T)}{n\pi(t_r/T)}\right)$$

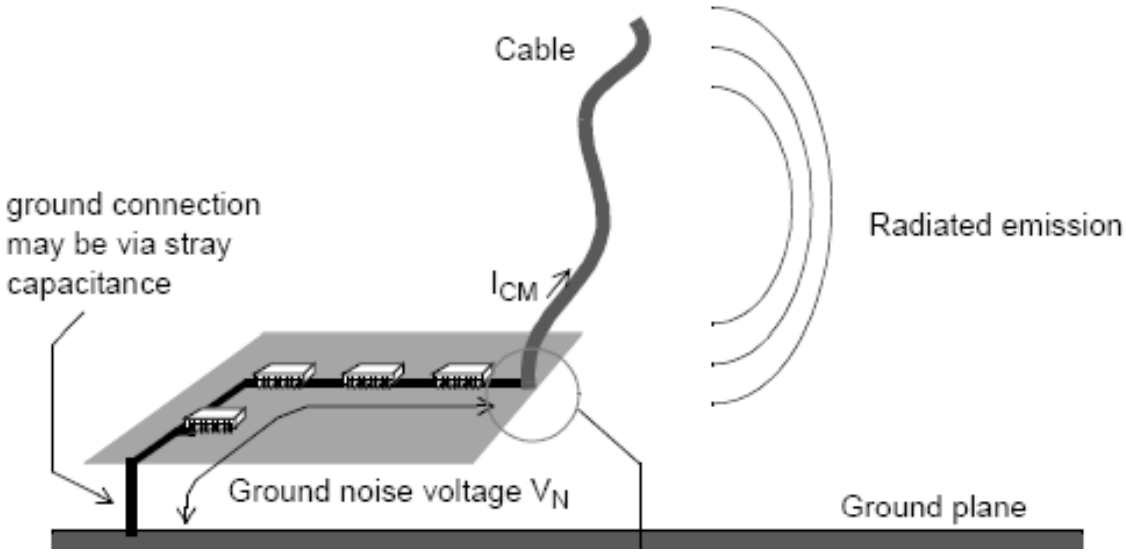
at the 5th harmonic current is 3.83mA.

Field strength limit : **E = 30dBμV/m,** and from **harmonic current 3.83mA, calculate** the allowable loop area "A" is

$$A \leqq 1.395cm^2$$

CM Radiated Emission

- $E = 1.26 \times 10^{-4} (f \times L \times I_{CM}) / R$ V/m



L: Cable length (m)

I_{CM} : CM Current (mA)

f : Frequency (MHz)

R: distance (m)

Signal Current cause EMI

- Emissions are caused by 『*Currents*』

  NOT *voltages*

  – In Maxwell's equations is also describe 『Current』 create H field, but NOT 『voltage』

- Most EMI emissions are caused by

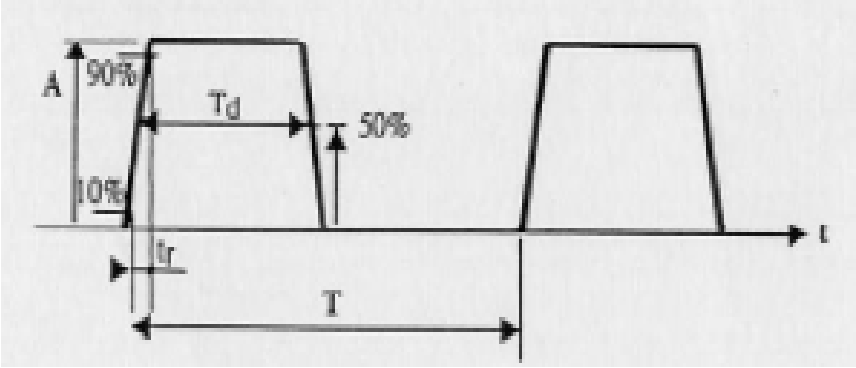
  『*Common Mode*』 currents

Intentional Signal Emissions

- Common Mode
  - Return Current does not ALL return directly under trace
  - Return current spread can affect entire board
  - Displacement current

What element cause Emission

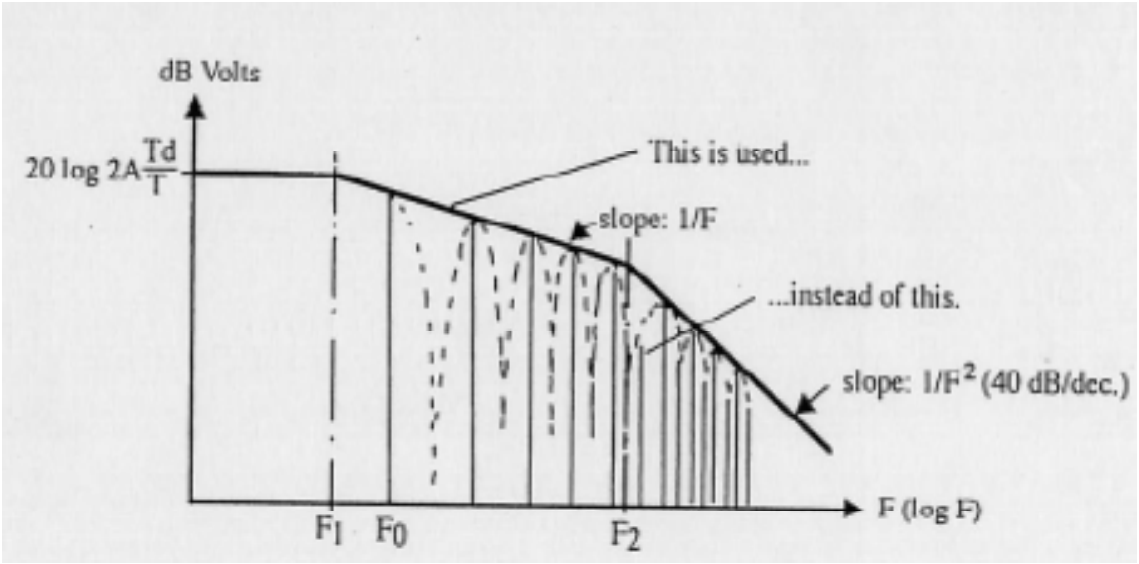
- Current : 『di/dt』
- bit rate
- rise time



$$F1 = \frac{1}{\pi Td}$$

$$F0 = \frac{1}{T}$$

$$F2 = \frac{1}{\pi Tr}$$



Concern Emission on PCB

- What shall we concern ??

Always concern Current Return Path!

Technical concept on PCB

- The concept of Current return path is very important to :
  - PCB design and Circuit Layout.

- Reduce EMC problem :
  - First method is “Control Current Return Path” on PCB

Concept 1

- Question #1. 

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  Current always return to….??

  - To Ground ??

  - To power /battery negative ??

  - To their source !!!

Which path will return current follow?

Figure A

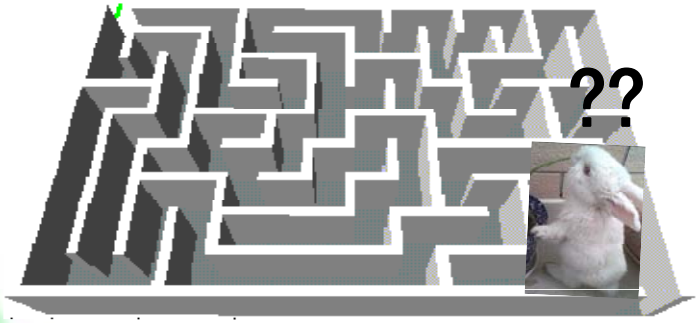
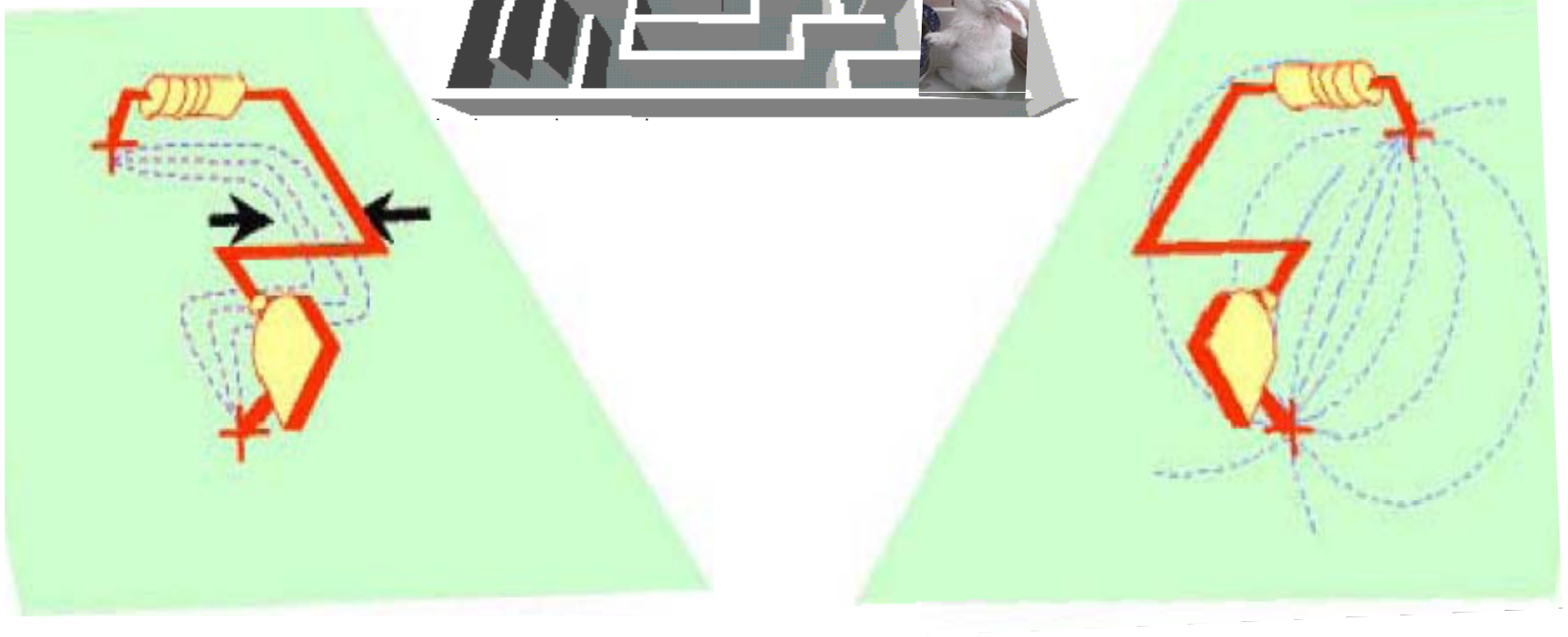


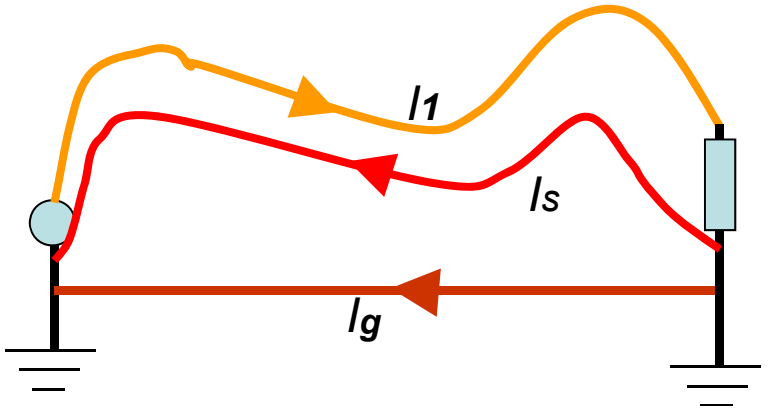
Figure B



Concept 2

Currents always take the path of least …

- Distance?
- Resistance?
- Inductance !!!

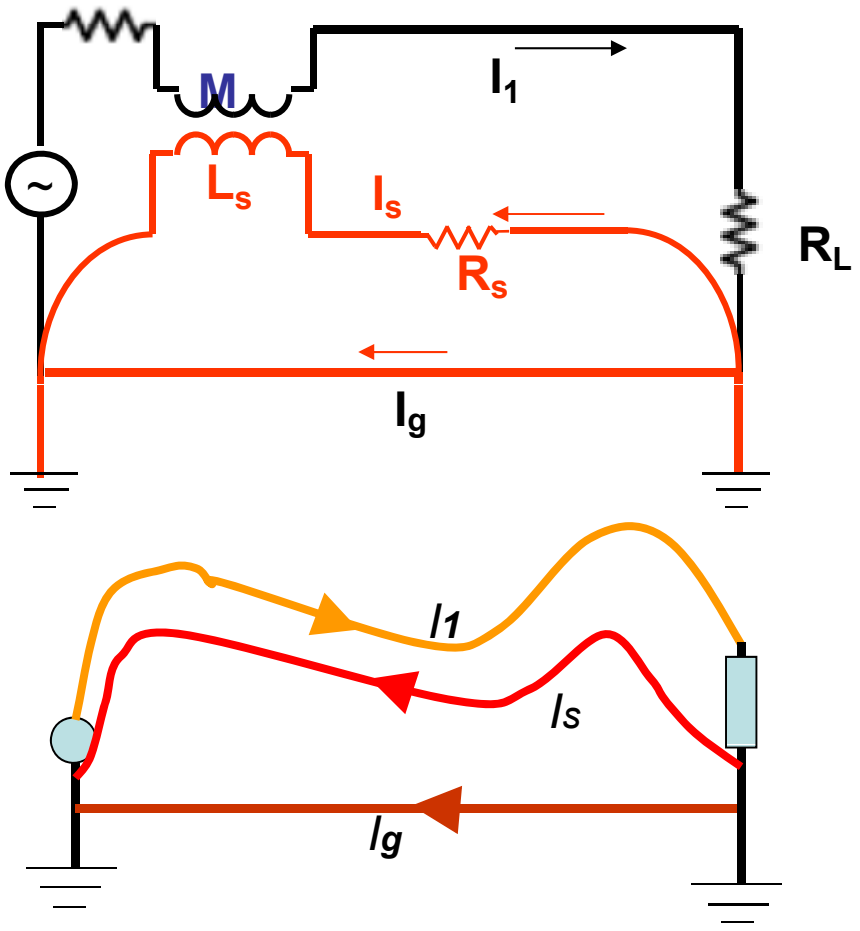


Inductance

- Inductance is associated with current
  - "Impedes" changes in current
- Inductance is a property of loops
- Even small inductances can be important

"$Z = j\omega L$"

Current Follow Analysis



$$Is\cdot(Rs+ j\,\omega\, Ls) - I_1\cdot J\omega M = 0$$

$$M = Ls \Rightarrow Ls = \frac{\mu}{2\pi} Ln\left(\frac{4H}{d}\right)\cdot\cdot \text{Hy/m}$$

$$\frac{Is}{I_1} = \frac{j\,\omega\, Ls}{Rs + j\,\omega\, Ls}$$

⇩

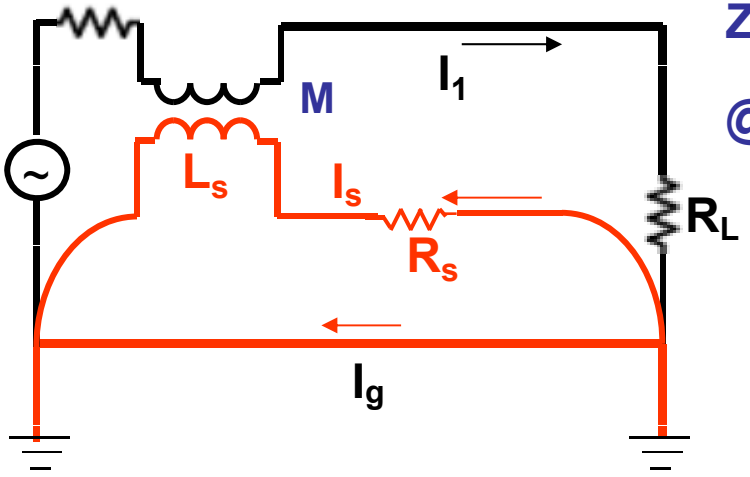
High frequency ω increasing

$$I_s \fallingdotseq I_g$$

Least Inductance on Path

- At high frequencies

Above 1 MHz (in typical copper structures), the current will follow the path of 『Least inductance』, via the return conductor (I_S)



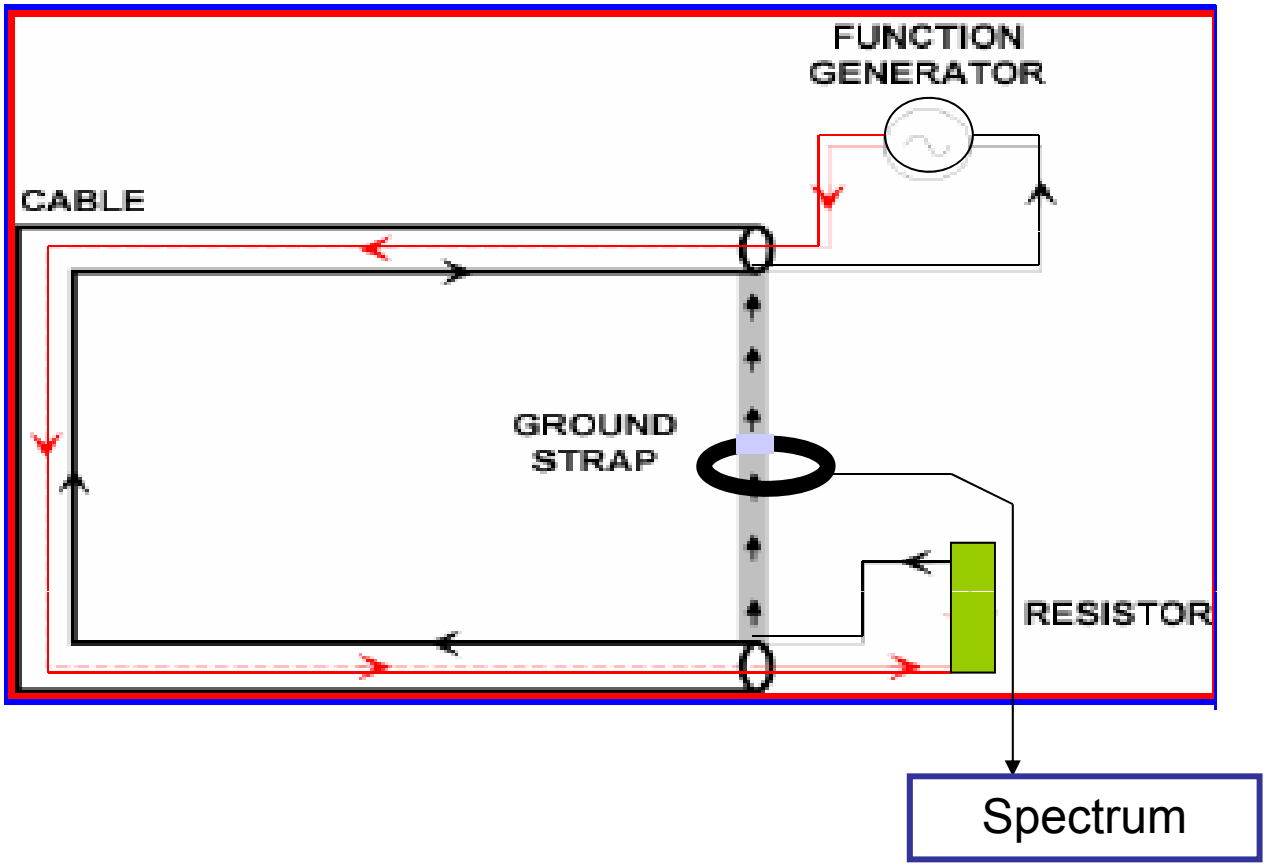
$$Z = Rs + j\omega M = |Z| \fallingdotseq \omega Ls$$

@ ωLs>>Rs

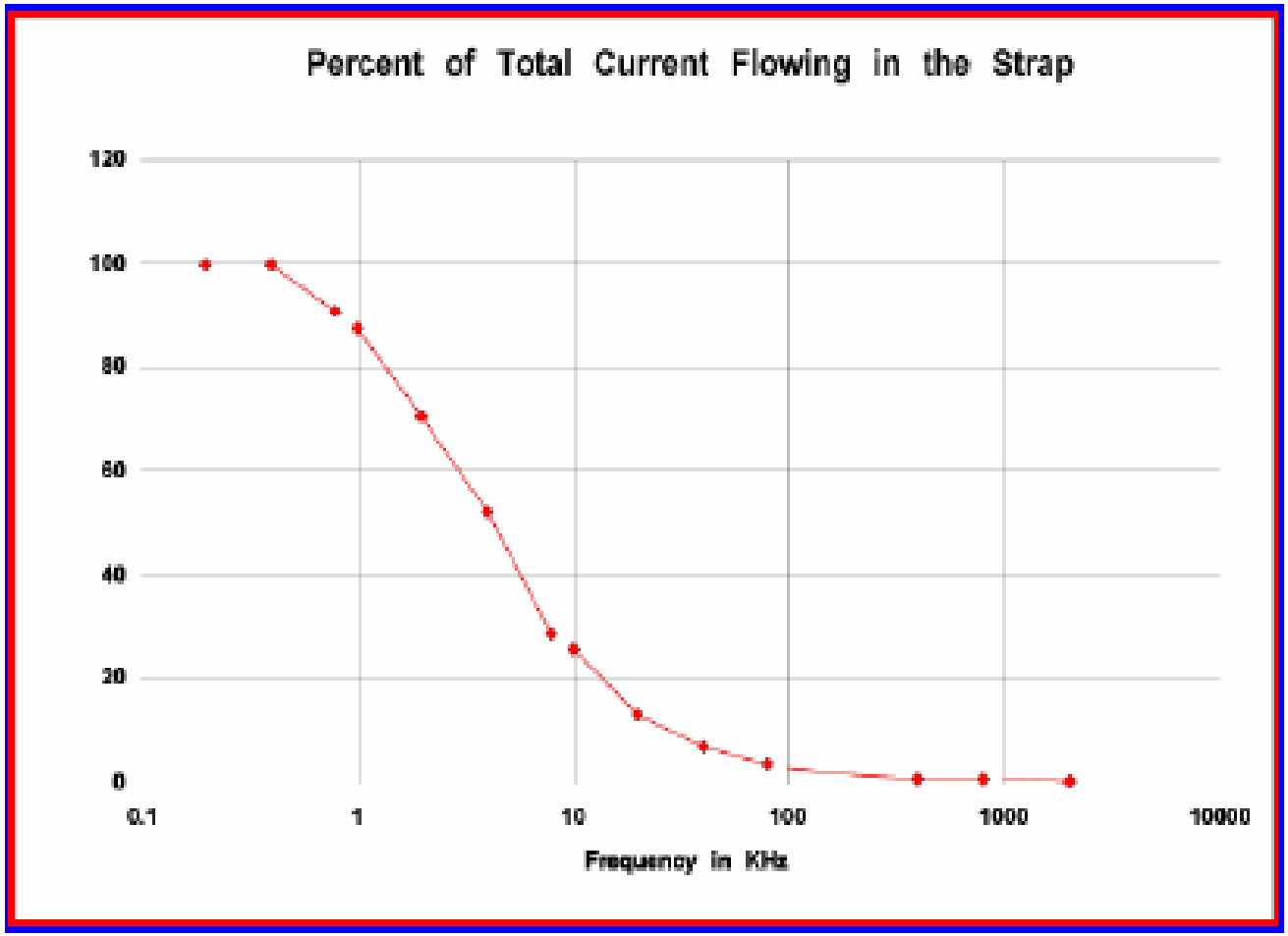
$$I_S = I_1 \cdot \frac{j\omega}{(j\omega + Rs/Ls)} \Rightarrow \fallingdotseq 1$$

Return current path observation

Experiment configuration



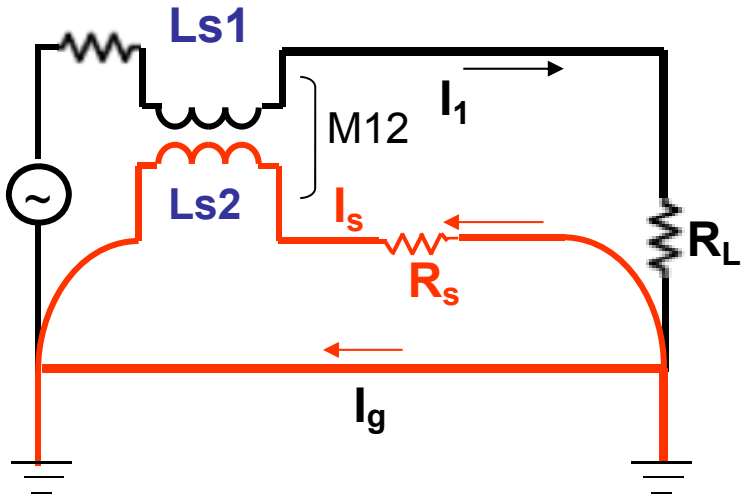
Result of current path



Current through low inductance

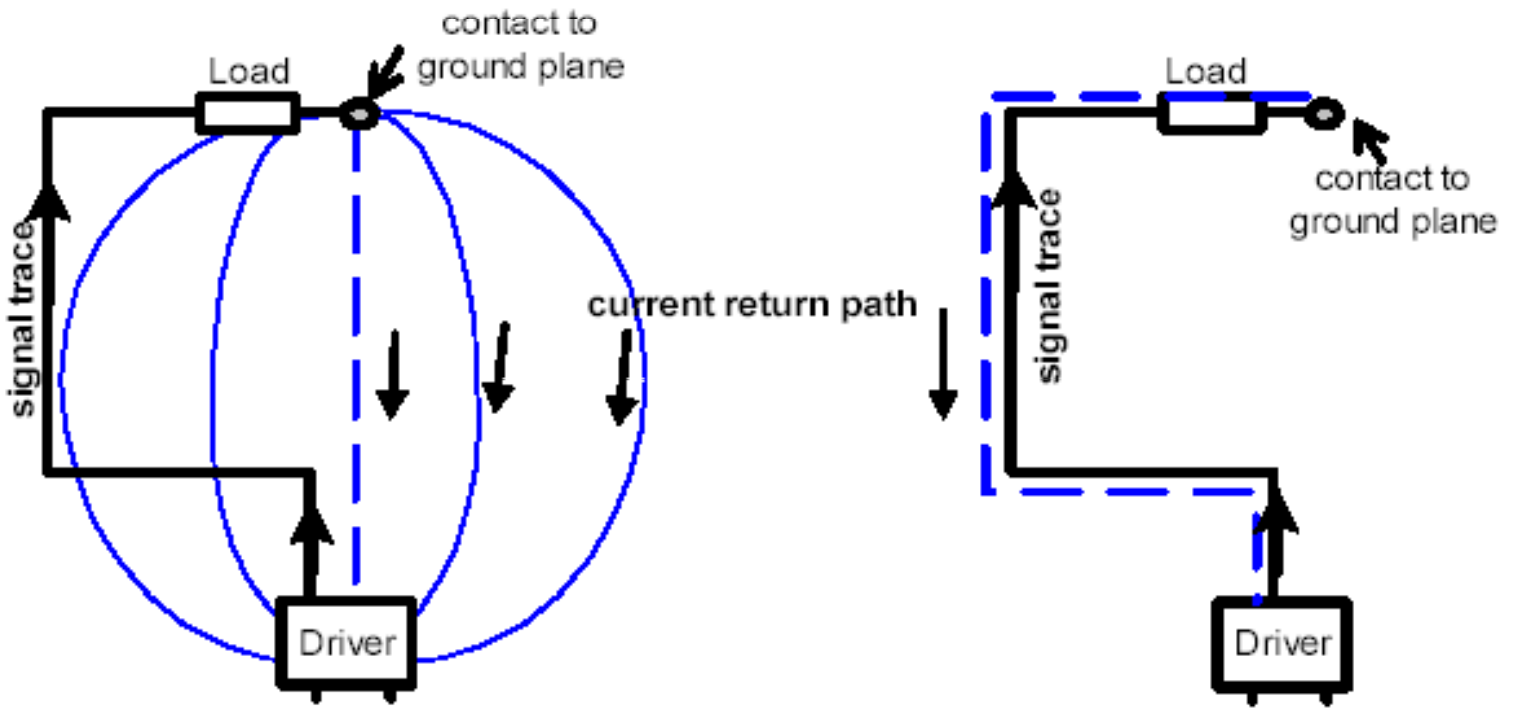
- Inductance is defined by the magnetic flux and current through a loop

$$L = \frac{\Psi_{loop}}{I_{loop}} = \frac{\int_S \vec{B} \cdot d\vec{S}}{I_{loop}}$$



- The total inductance of two carry current in the loop of (signal & return leads)
- **$L_{total} = Ls1 + Ls2 - 2M_{12}$**

Current Path of least Inductance

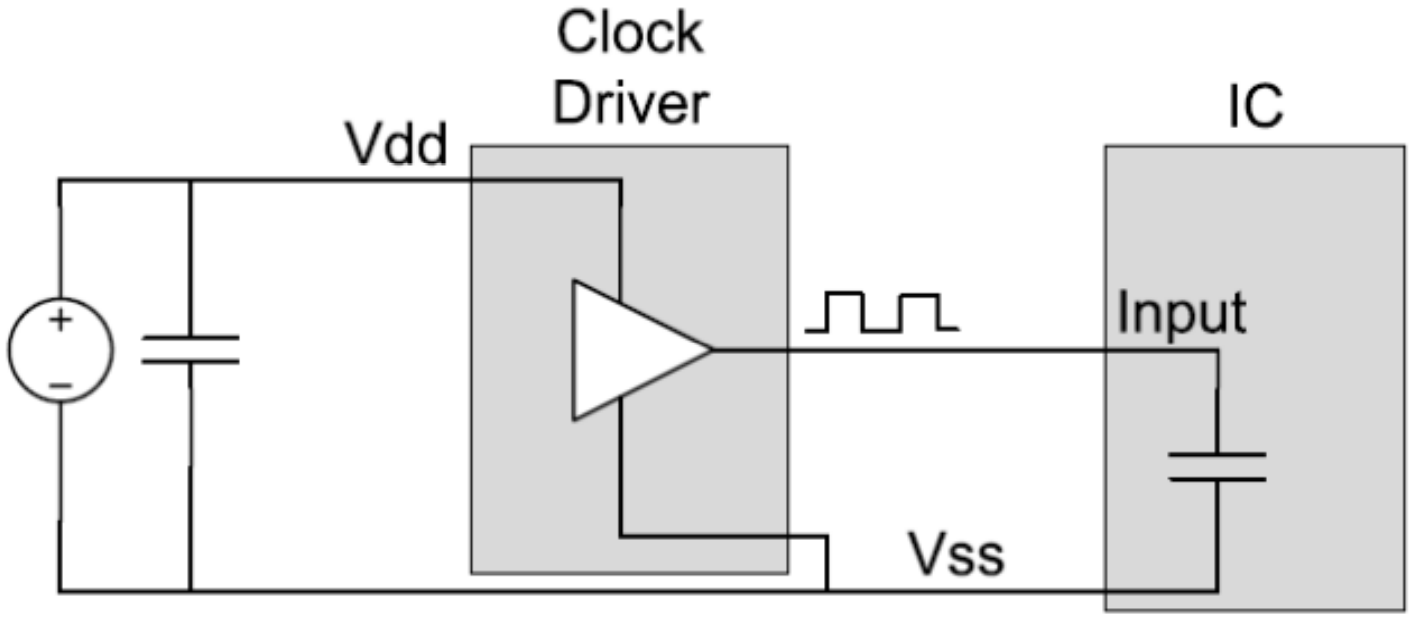


Low speed signal trace over ground plane. Current return path of least resistance

High speed signal trace over ground plane. Current return path of least inductance

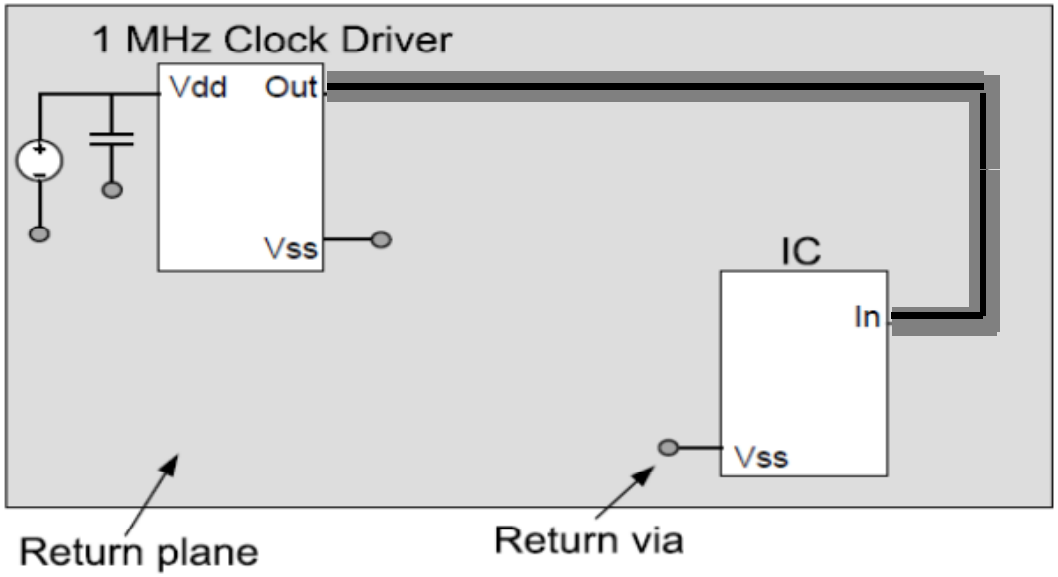
Current return path

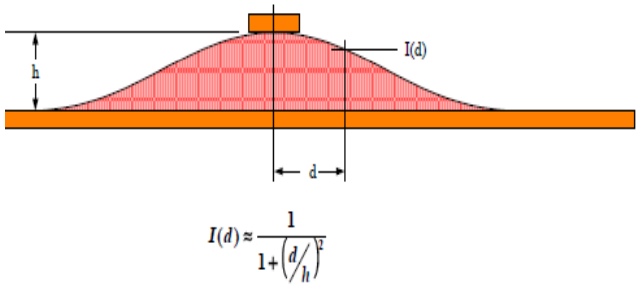
- Current always returns to its source



High-frequency return current path

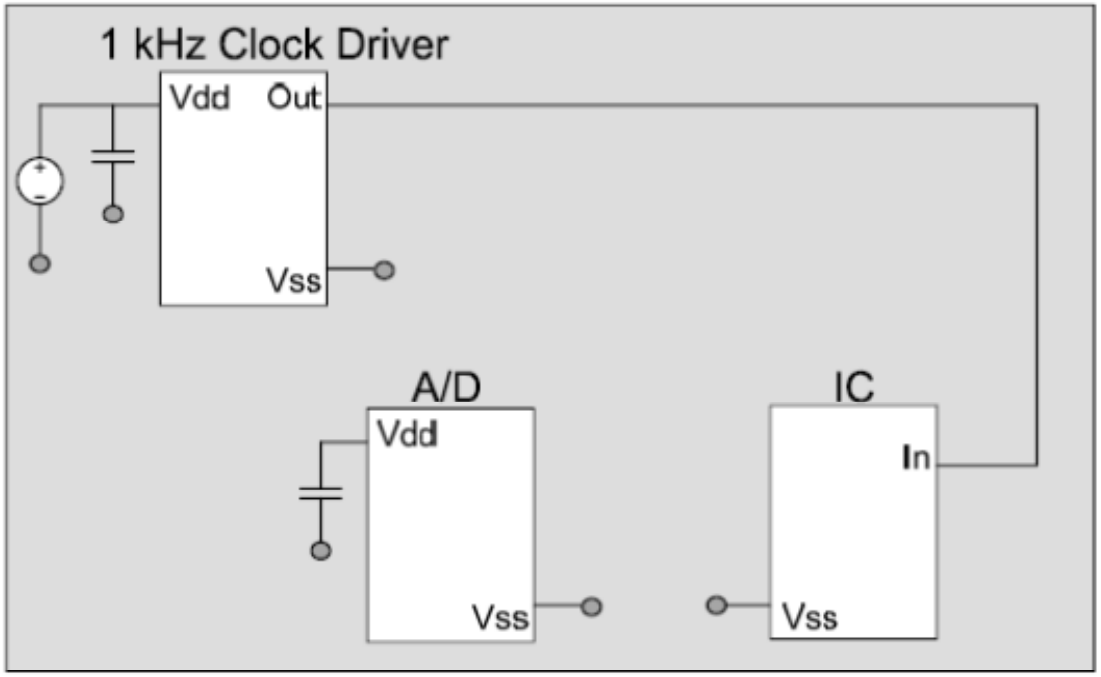
- High frequency return current always flows close to the signal trace.

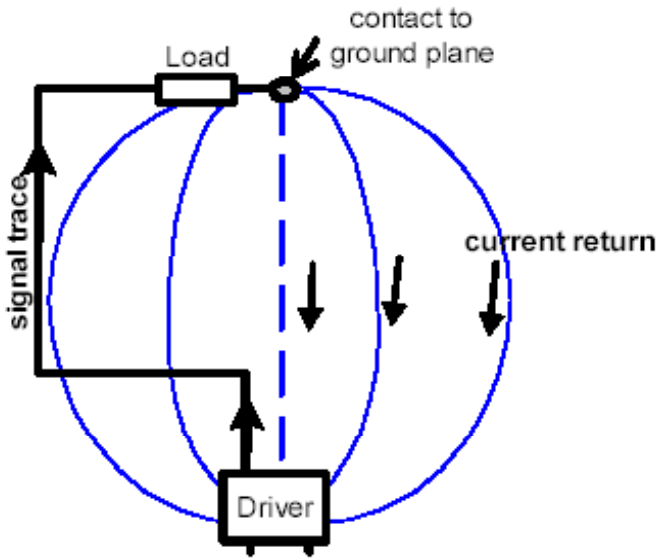




low-frequency current return path

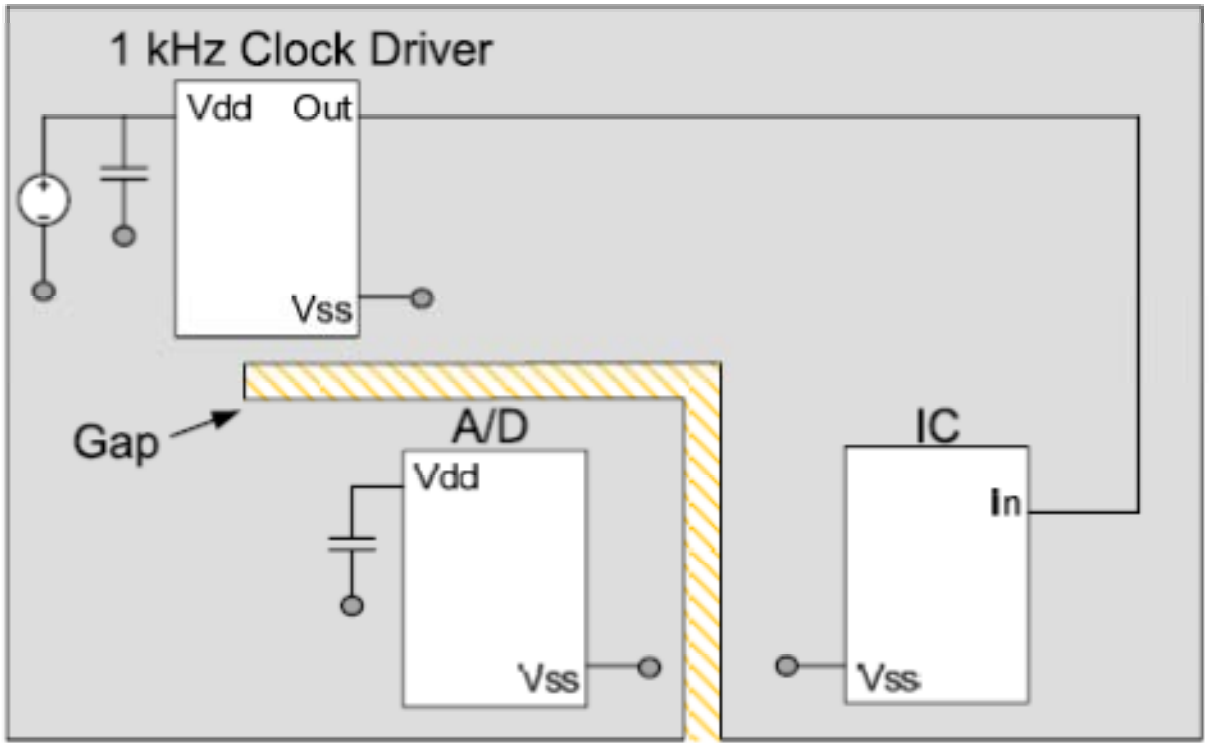
- Low frequency return current spreads across the whole plane.
- Return current may cause interference





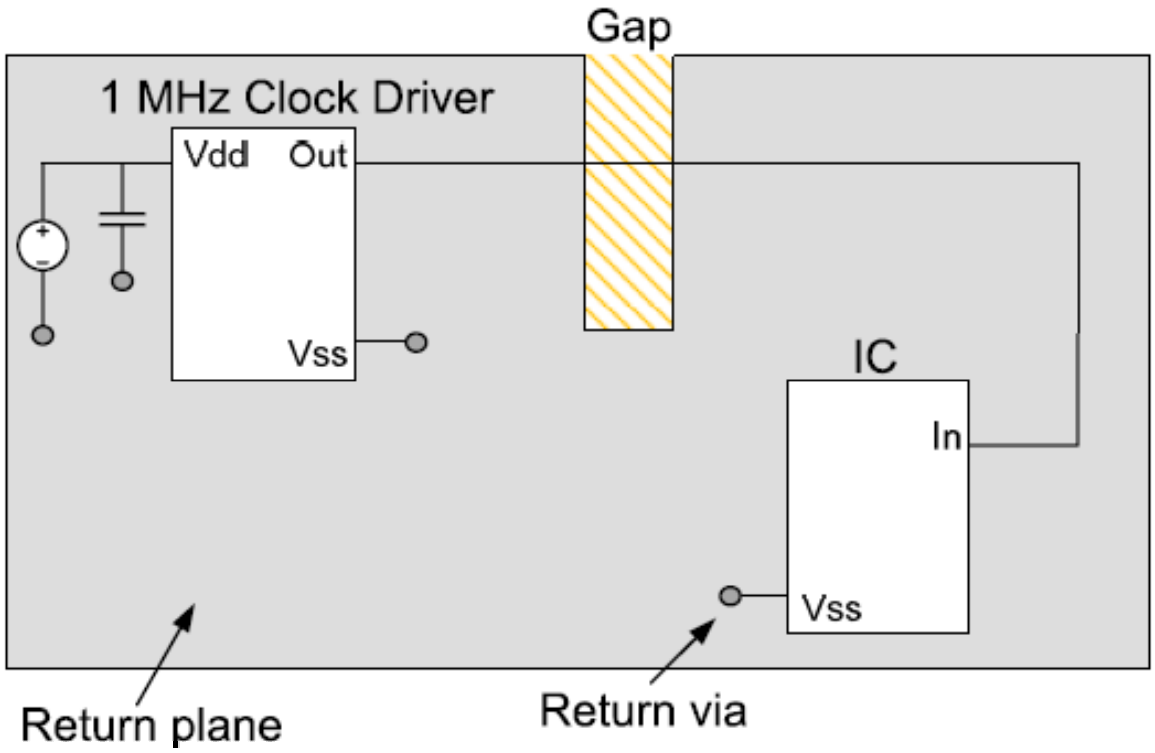
Use a gap in plane to isolate components?

- Gapping the return plane should be avoided.



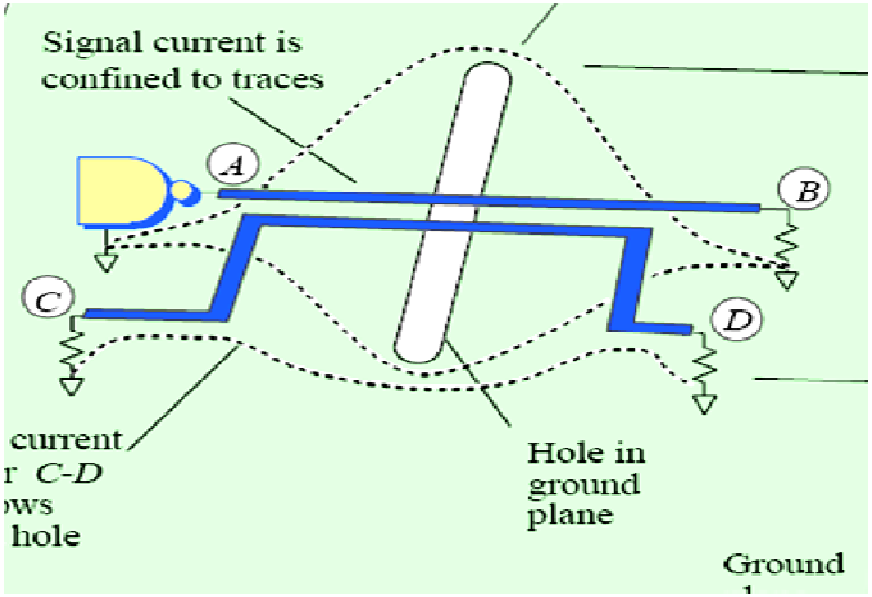
Avoid crossing gaps with traces

- Crossing the gap may cause emission



Trace over reference plane

- When the Reference Plane is not perfect
  - Splits in power plane?
  - What happen when traces across split?



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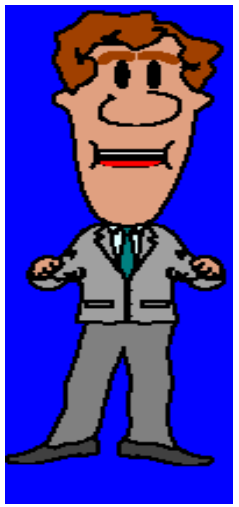
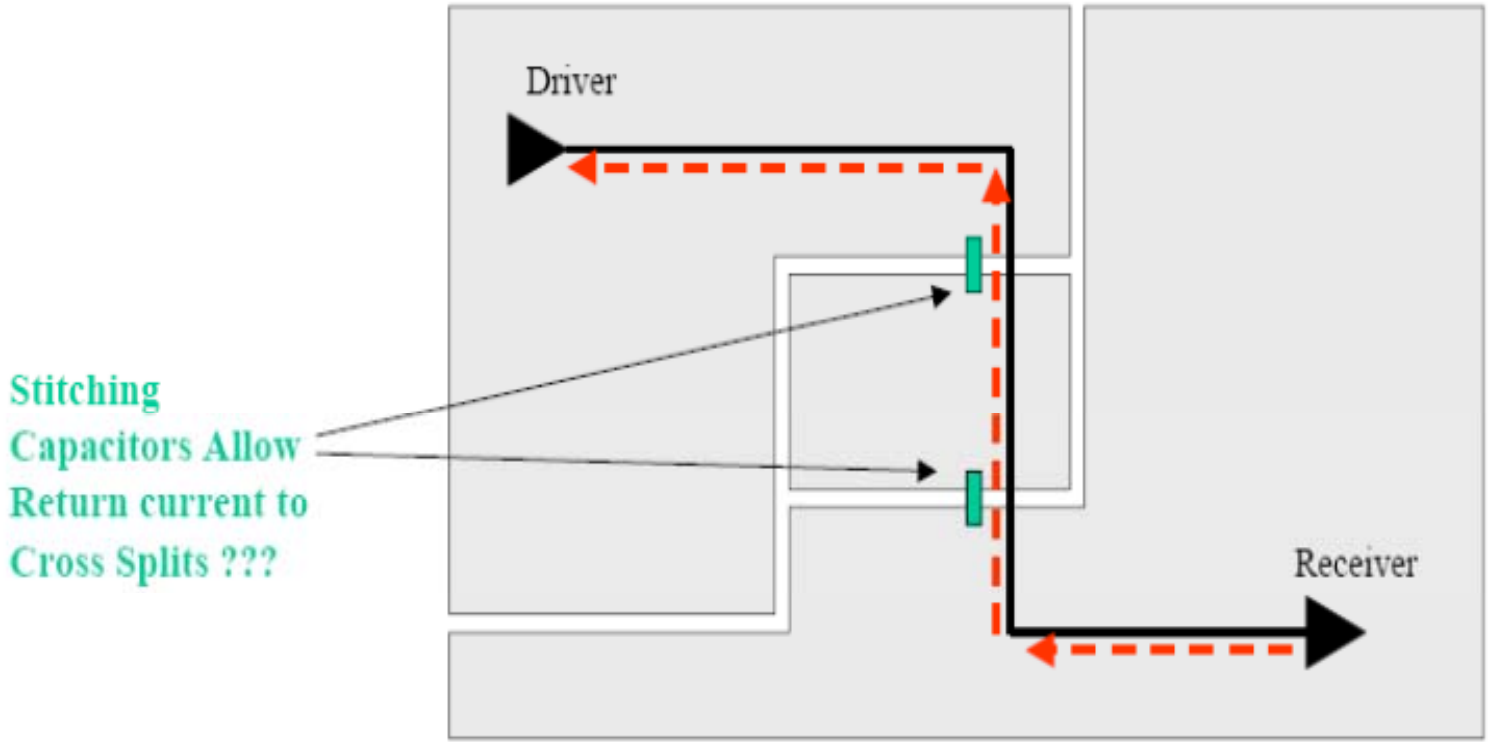
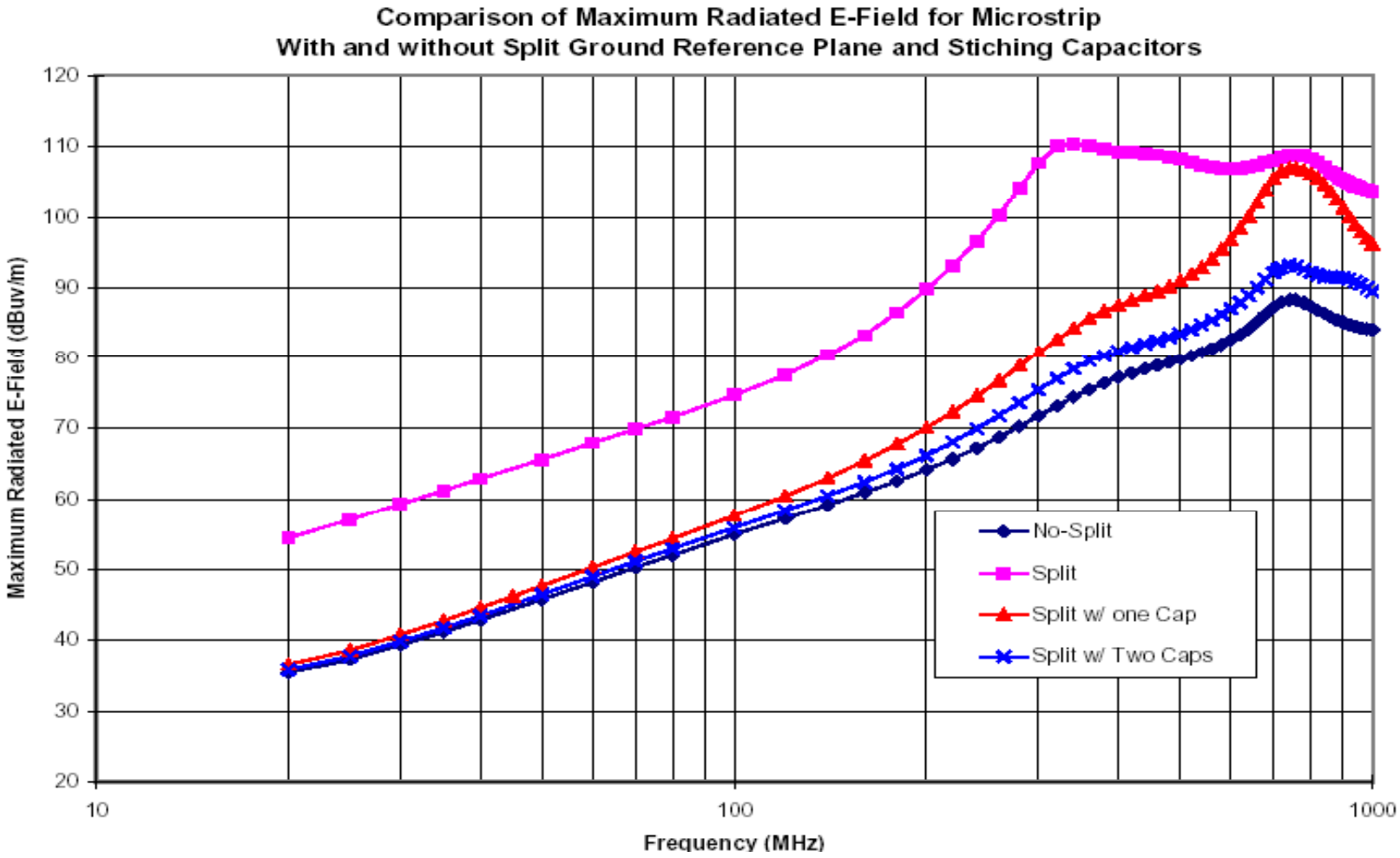


Split Reference Plane Example

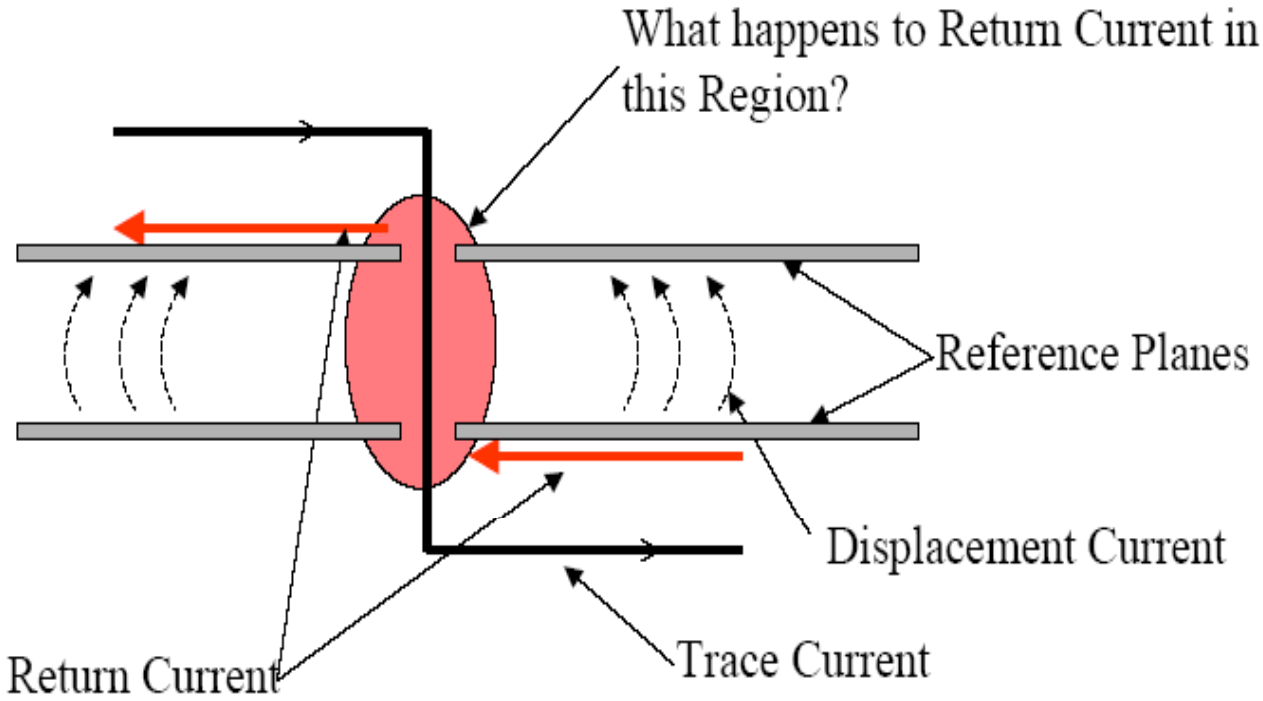


With "Perfectly Connected" Stitching Capacitors Across Split

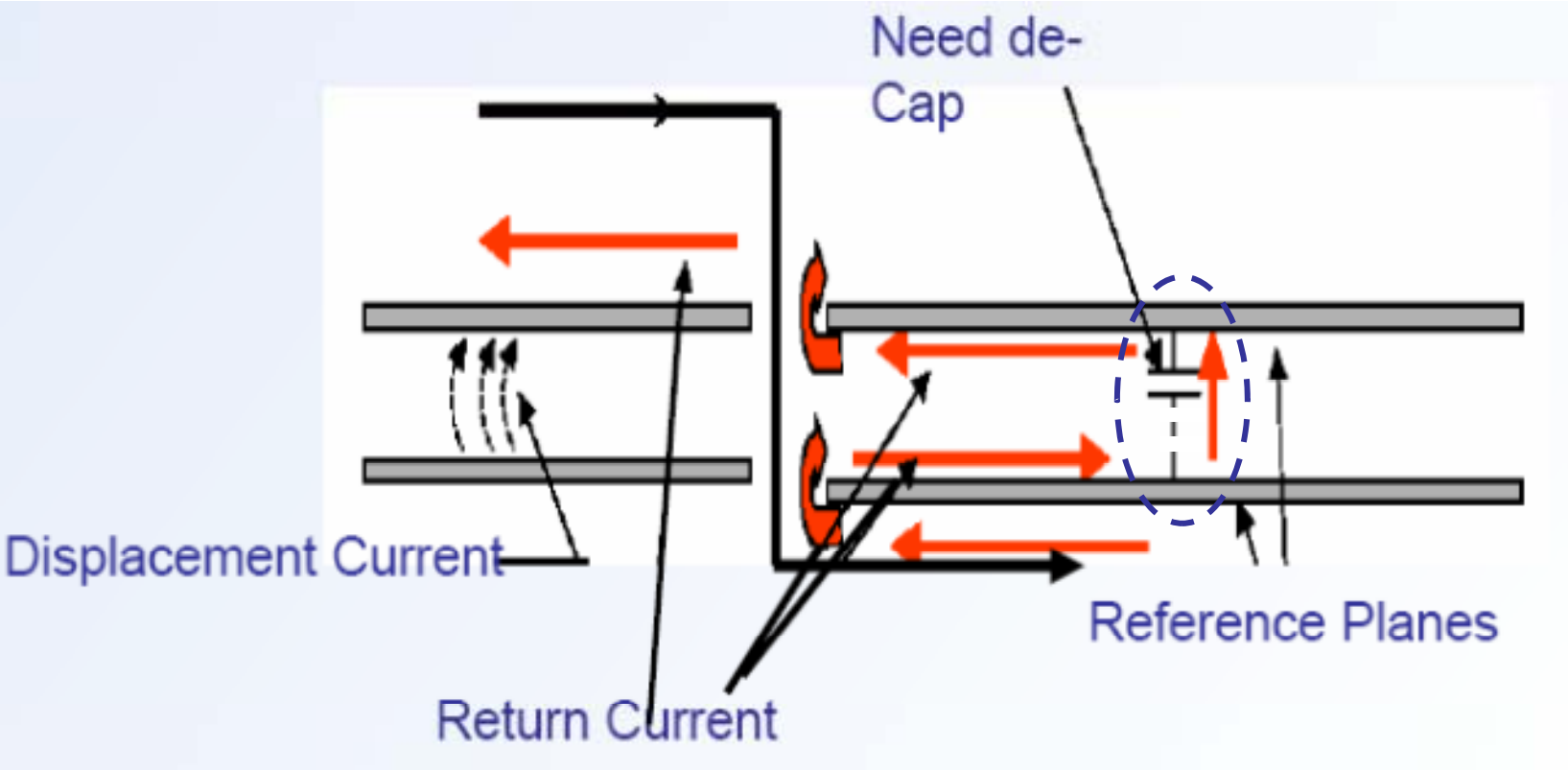


Return Current Across Reference Plane

Use displacement current between planes

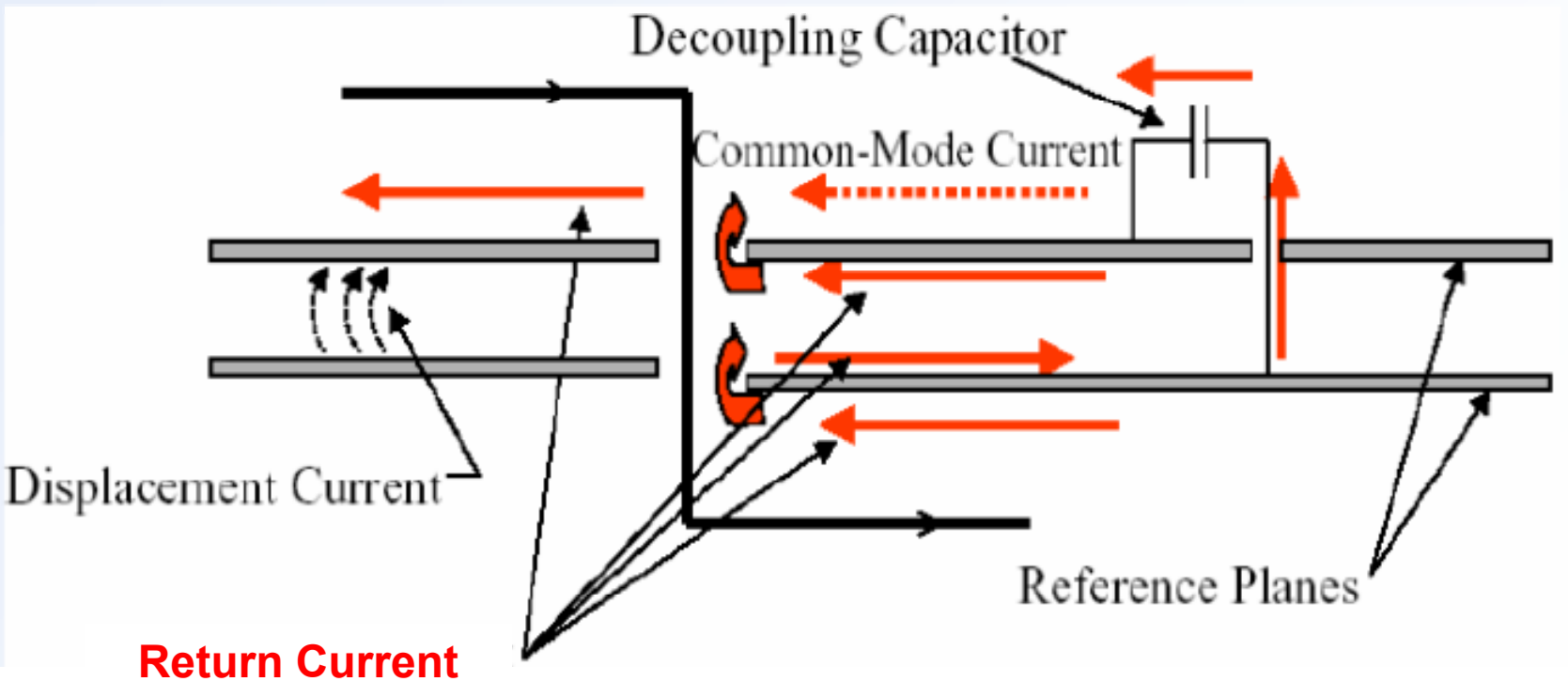


Return Current Flow When Signal Line Goes Through Via

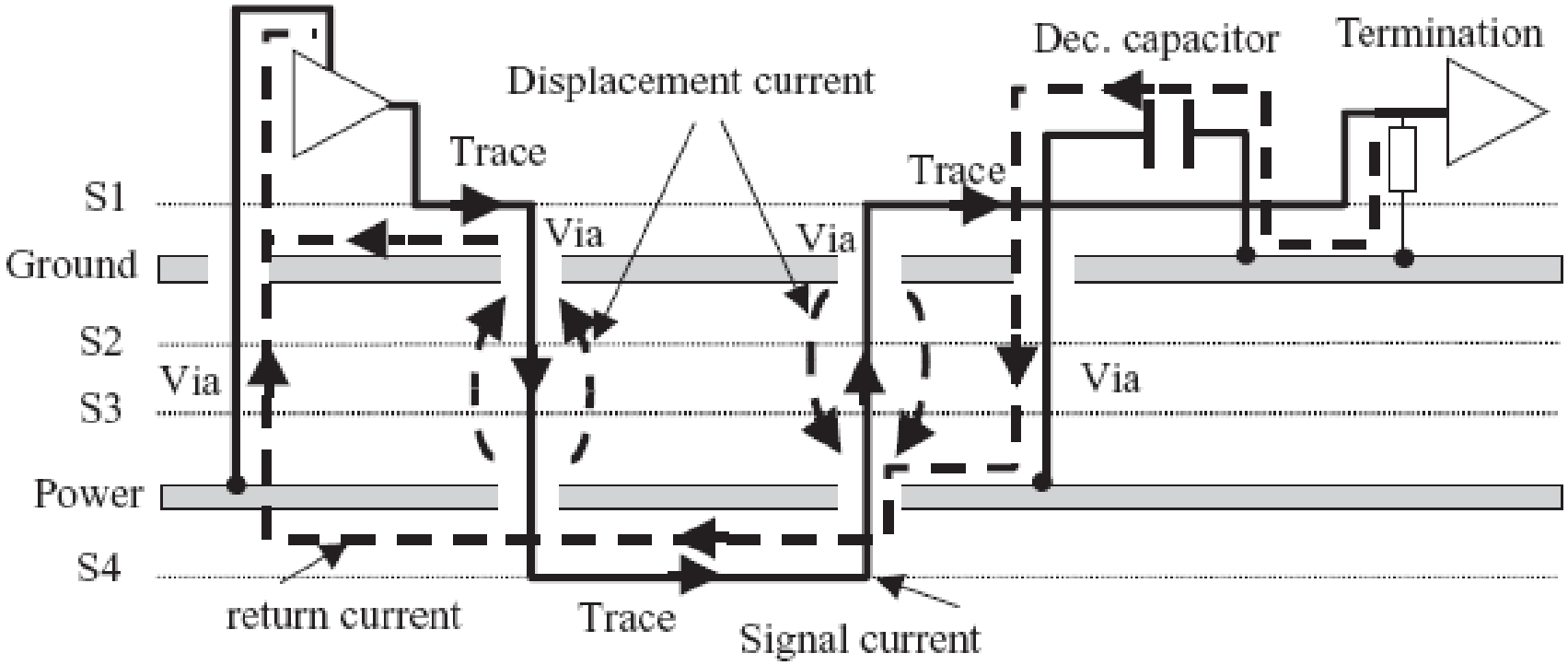


Change Reference Plane

With Decoupling Capacitor (on Top)



Signal and return current path in a multi-layer PCB.

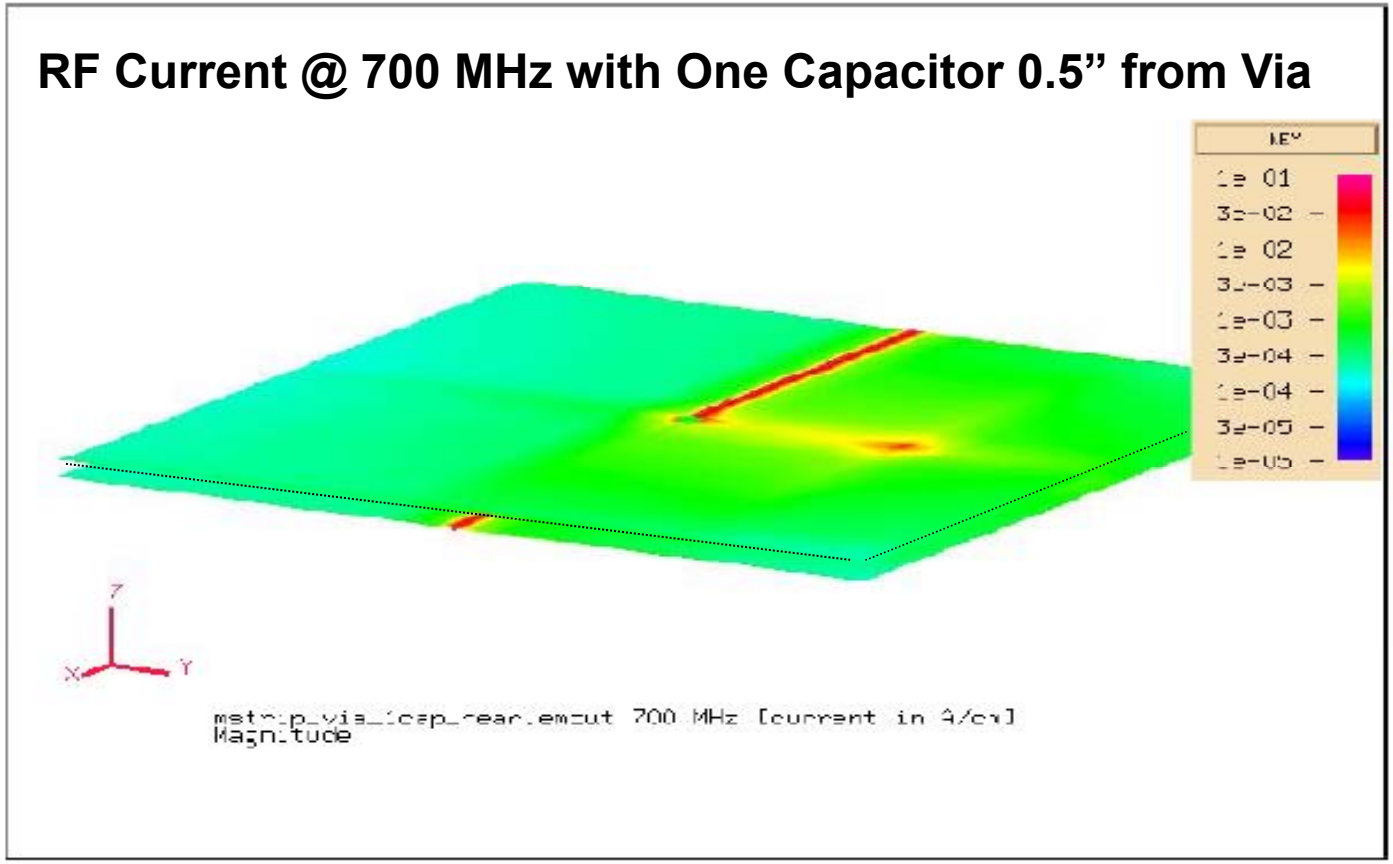


Location of Decoupling Capacitors

Relative to Via is Important!

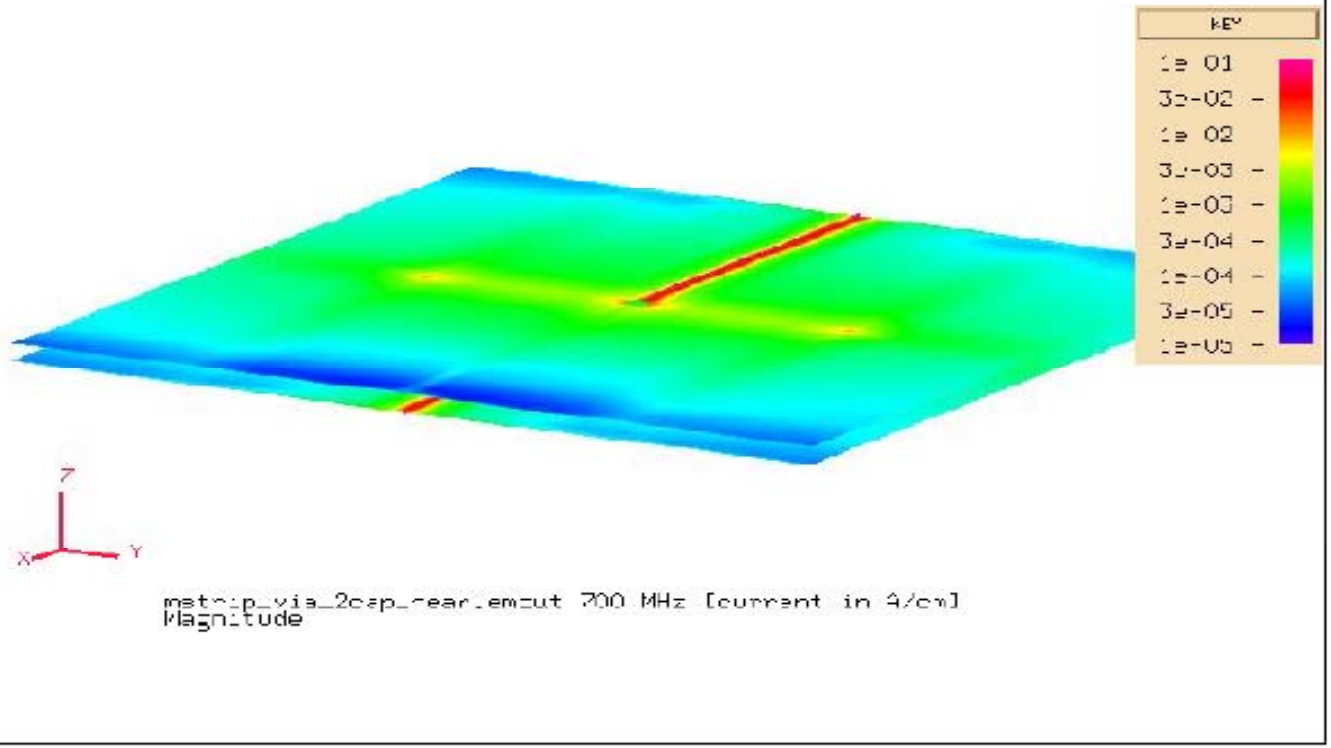
- One Decoupling Capacitor at 0.5”
- Two Decoupling Capacitors at 0.5”
- Two Decoupling Capacitors at 0.25”

Example of RF emission from via on reference plane (1)



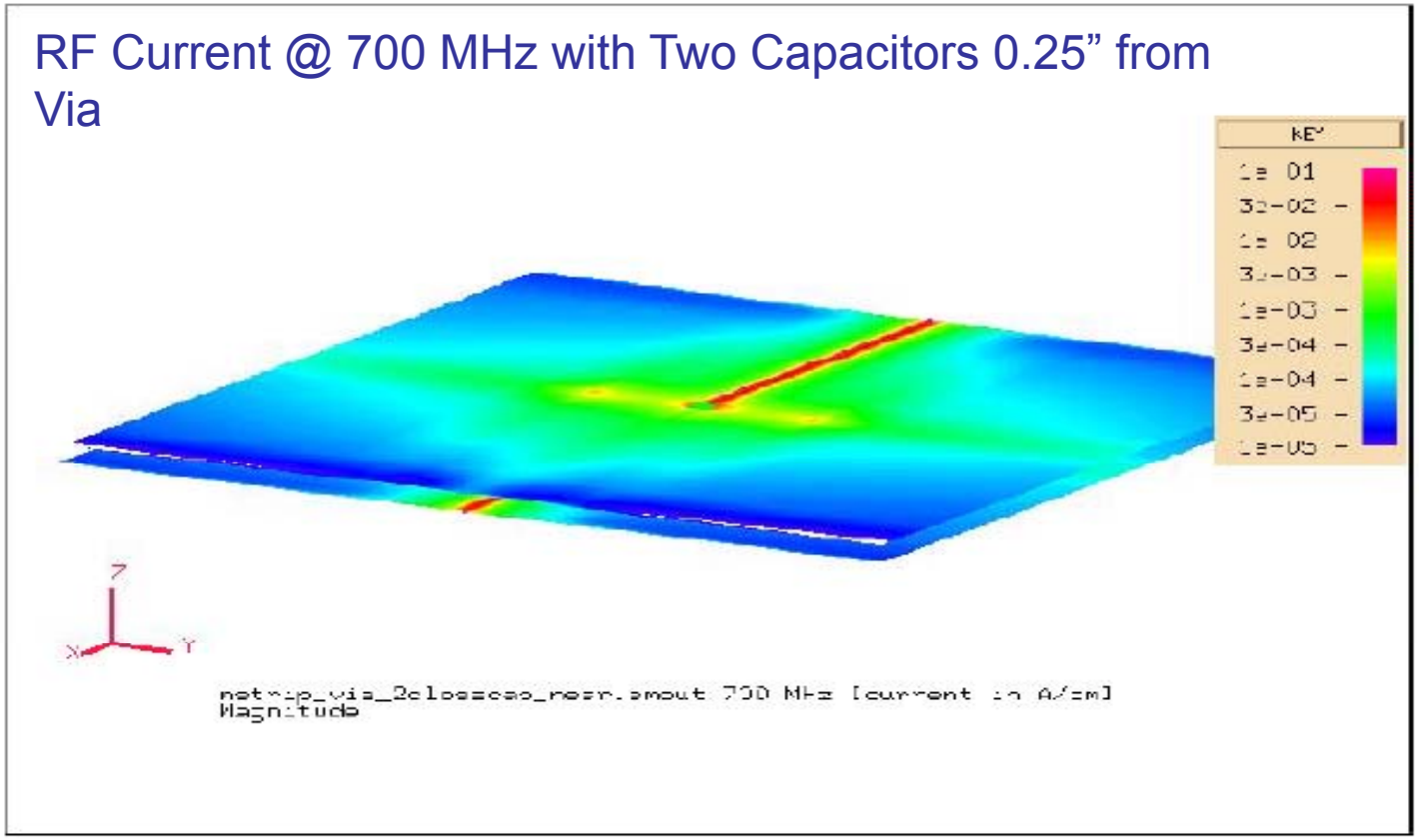
Example of RF emission from via on reference plane (2)

RF Current @ 700 MHz with Two Capacitors 0.5” from Via



Example of RF emission from via on reference plane (3)

RF Current @ 700 MHz with Two Capacitors 0.25” from Via



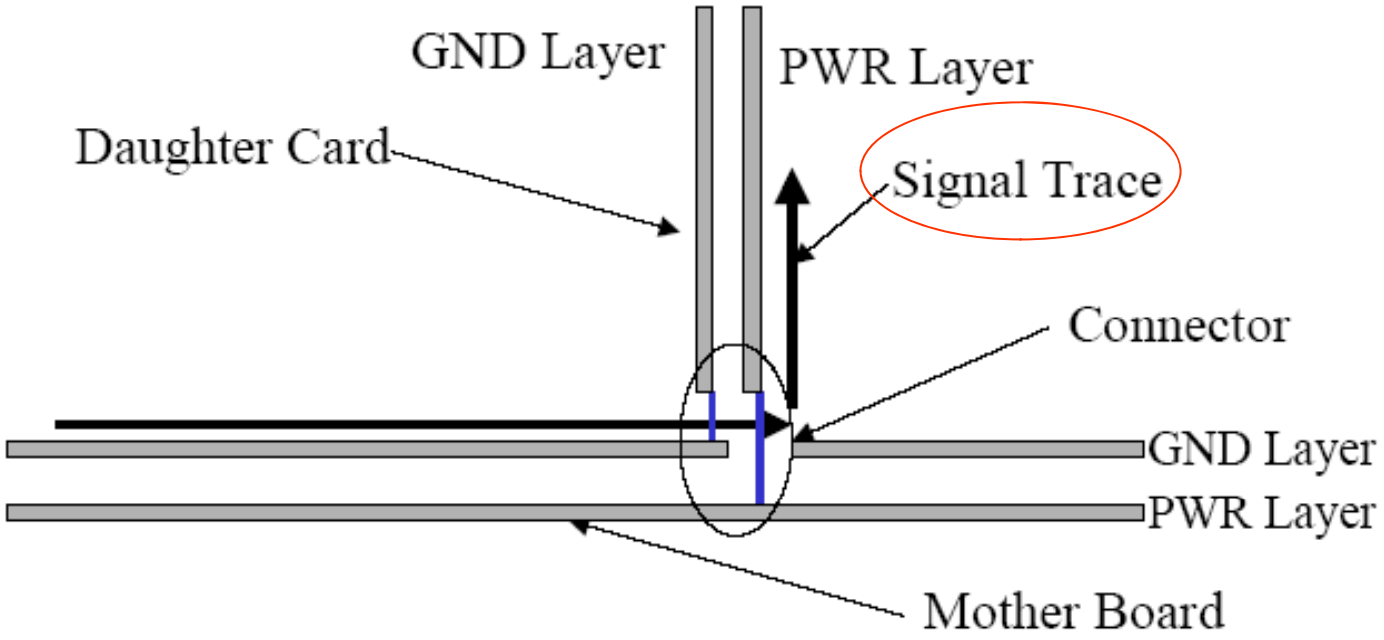
Common Mode Current

- Basically, current where we never intended it to be!
  - Return current spread under trace.
  - Return current path when trace cross over split in reference plane.
  - Return current path when traces go through a via and changes reference planes.

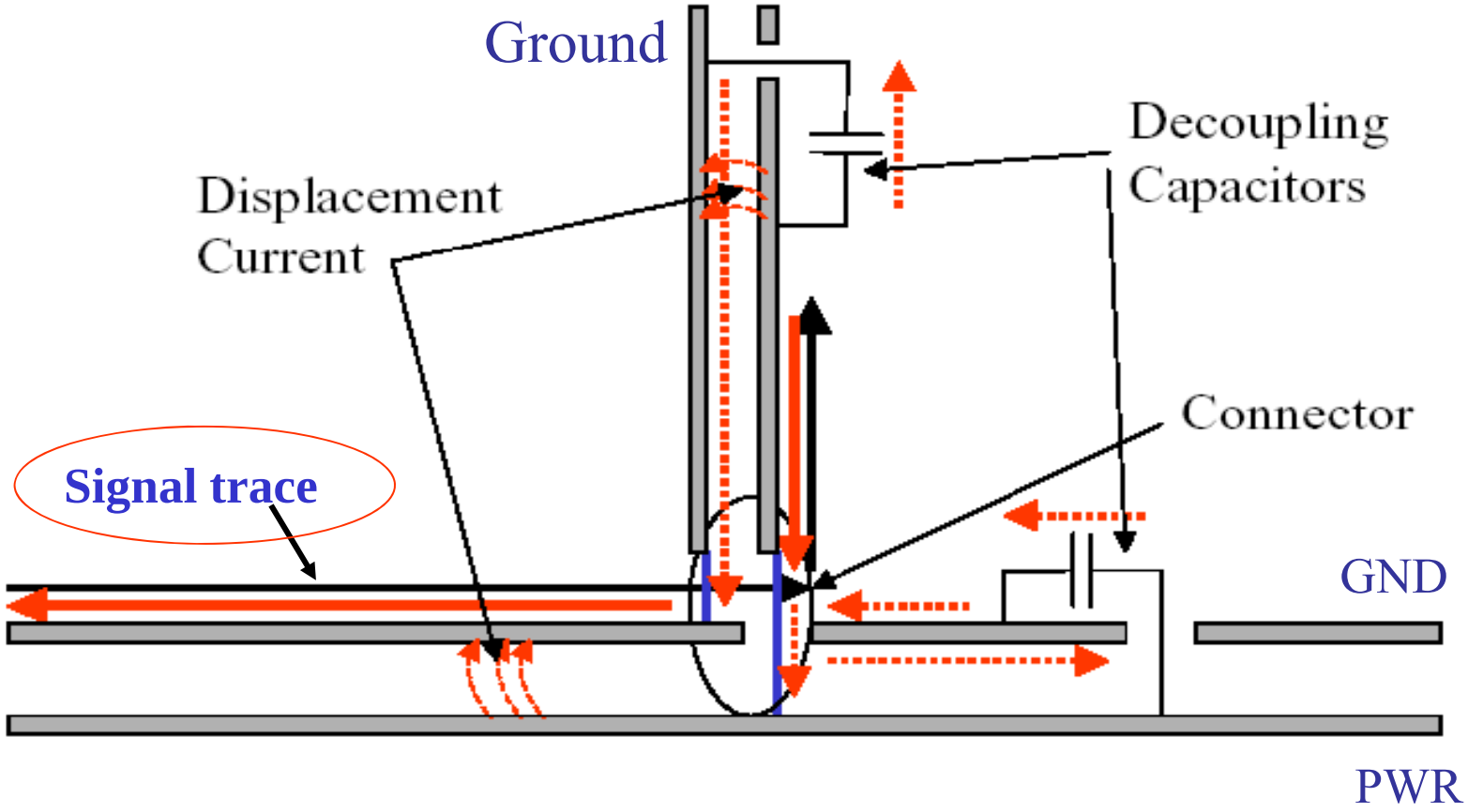
Important

- Current leaves a driver on a trace and must return (somehow) to its source
- this seems basic, but it is often forgotten, and is most often the cause of EMC problems
- Ground-Reference Decoupling is still needed

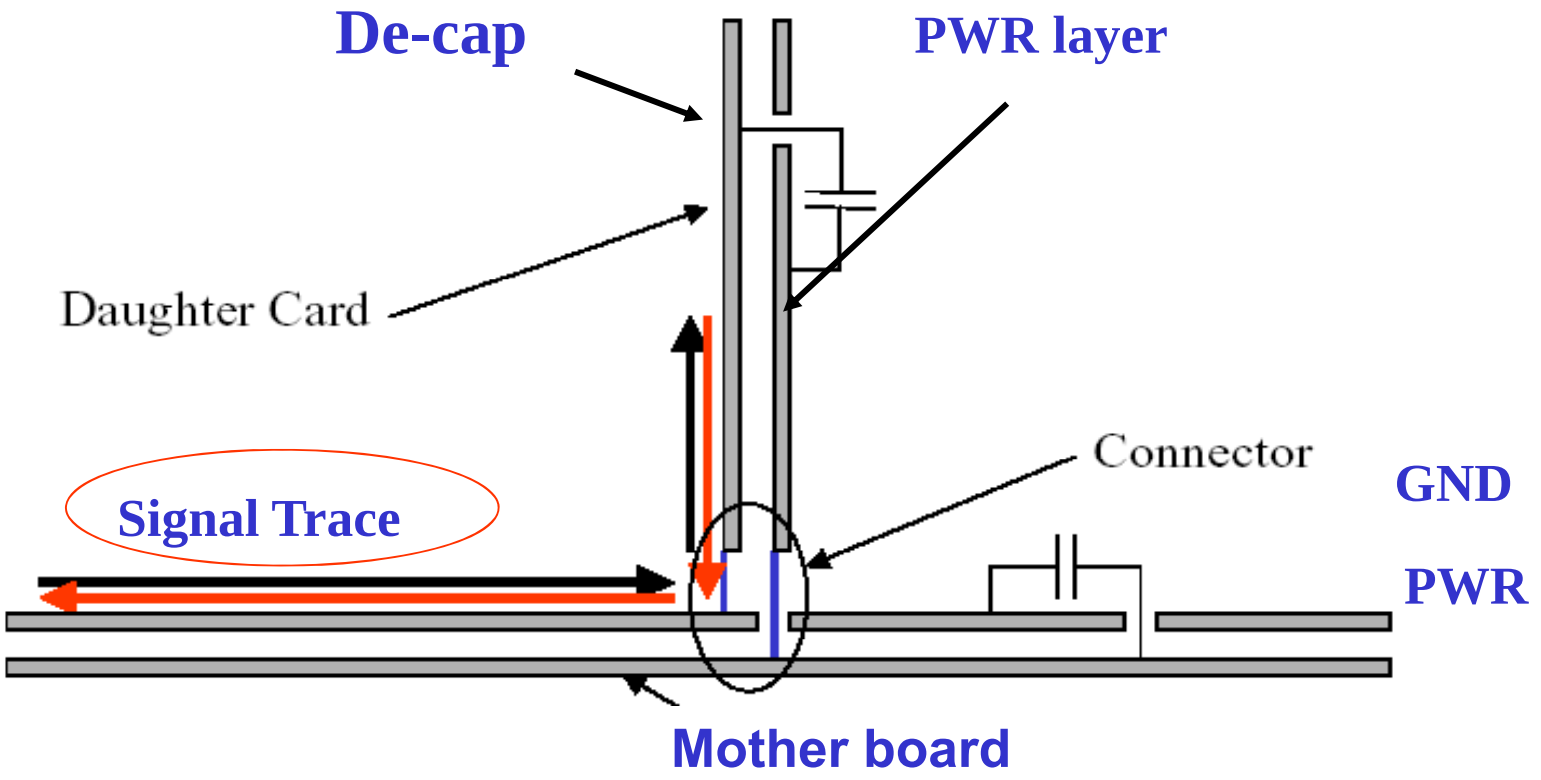
Mother / Daughter Board Connector Crossing



Return Current from Improper Referencing Across Connector



Return Current from Proper Referencing Across Connector



Summary

- Intentional signal ***return current di/dt*** cause EMI emission.
- Important Things is 『Control the **current return path**』
- Consider 『Displace Current』 cause separately
- Using decoupling capacitor to minimize Displace current separate area.

Summary

- Route Critical Traces first.
- Consider EMC effects *early* during board design
- Lower Loop inductance
- USB and Ethernet special cases
  - don’t need planes under final I/O lines.

Thank you for attendance